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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,380	11/30/2004	Toshiki Makimoto	14321.63	2860
22913	7590	11/01/2007	EXAMINER	
WORKMAN NYDEGGER 60 EAST SOUTH TEMPLE 1000 EAGLE GATE TOWER SALT LAKE CITY, UT 84111			NGUYEN, TRAM HOANG	
			ART UNIT	PAPER NUMBER
			2818	
			MAIL DATE	DELIVERY MODE
			11/01/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

TH

**Office Action Summary**

Application No.

10/516,380

Applicant(s)

MAKIMOTO ET AL.

Examiner

Tram H. Nguyen

Art Unit

2818

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10/15/2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 50-60 and 77-85 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 50-60 and 77-85 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

In response to the communications dated 10/15/2007, claims 80-85 have been added. Therefore, claims 50-60, 77-79 and 80-85 are pending in this application.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

***Claims 50-60 and 77-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makimoto (US 2002/0195619; hereinafter Makimoto); further in***

***view of K. Kumakura, T. Makimoto and N. Kobayashi, Low-Resistance Nonalloyed Ohmic Contact to p-type GaN Using Strained InGaN Contact Layer, Applied Physics Letters, Vol. 79, No. 16, pp 2588-2590 (2001).***

Regarding **claim 50**, Makimoto disclose a nitride semiconductor structure (fig. 10) comprising: on a substrate (item 101); an n-type collector layer (item 104); a p-type base layer (item 106) formed over said n-type collector layer (104); and an n-type emitter layer (107) formed over said p-type base layer (106).

Fig. 10 of Makimoto shows an Pd/Au layer (109) formed on the exposed top surface of the p-type base layer (106)

Makimoto fails to teach an indium-containing p-type nitride layer formed on a surface of said p-type surface, the top surface having been exposed by etching said n-type emitter layer; a base electrode formed on the indium containing p-type nitride semiconductor layer.

However, Kumakura et al. suggests forming a p-type InGaN layer directly on between a metal Pd/Au layer and a p-type GaN (see pg. 2588 of Kumakura et al.: column 1, paragraph 2 and fig. 1). Therefore, it would have been obvious to one having ordinary skills in the art at the time the invention was made to insert a p-type InGaN contact layer between Pd/Au and p-type GaN as taught by Kumakura et al. in the device structure of Makimoto in order to improve the device performance by reducing the resistance contacts (see Mumakura et al.: pg. 2588; column 1, paragraph 2).

The limitation “the top surface having been exposed by etching said n-type emitter layer” (as noted in lines 7-8 of claim 50) refers to a product by process claim is

directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck 177 USPQ 523; In re Fessman 180 USPQ 324; In re Avery 186 USPQ 161; In re Wertheim 191 USPQ 90; and In re Marosi et al 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process claim, and not the patentability of the process, and that an old product produced by a new method is not patentable as a product, whether claimed in "product by process claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding **claim 51**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Mumakura teaches said p-type nitride semiconductor layer (refer to the p-type InGaN formed between Pd/Au and p-type GaN) is p-type InGaN.

Regarding **claim 52**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Fig. 10 of Makimoto shows said p-type base layer is p-type InGaN (106).

Regarding **claim 53**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type InGaN base layer has an indium mole fraction of 5-30% (see fig. 10 exhibits the p-type InGaN base containing 6% of Indium).

Regarding **claim 54**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. The combination of Makimoto and Mumakura teaches said p-type nitride semiconductor layer (according to Mumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 55**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type base layer is p-type InGaN (see claim 52's rejection).

Regarding **claim 56**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type InGaN base layer has an indium mole fraction of 5-30% (see claim 53's rejection).

Regarding **claim 57**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. The combination of Makimoto and Mumakura teaches said p-type nitride semiconductor layer (according to Mumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 58**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Makimoto teach said p-type InGaN base layer has an indium mole fraction of 5-30% (see claim 53's rejection).

Regarding **claim 59**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. The combination of Makimoto and Mumakura teaches said p-type nitride semiconductor layer (according to Mumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 60**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. The combination of Makimoto and Mumakura teaches said p-type nitride semiconductor layer (according to Mumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 77**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set forth above. Furthermore, Fig. 10 of Makimoto shows a graded layer (105) between the p-type base layer (106) and the n-

type collection layer (item 104); wherein the graded layer (106) has its indium mole fraction varied gradually (see par.[0009],lines 1-3).

Regarding **claim 78**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set forth above. Furthermore, Fig. 10 of Makimoto shows a graded layer (105) between the p-type base layer (106) and the n-type collection layer (item 104); wherein the graded layer (105) has its indium mole fraction varied gradually (see par.[0009],lines 1-3).

Regarding **claim 79**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set forth above. Furthermore, Fig. 10 of Makimoto shows a graded layer (105) between the p-type base layer (106) and the n-type collection layer (item 104); wherein the graded layer (105) has its indium mole fraction varied gradually (see par.[0009],lines 1-3).

Regarding **claim 80**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set forth above. As mentioned above, Mumakura et al. teach a heterojunction structure wherein placing the indium-containing p-type nitride semiconductor (refer to p-type InGaN layer) directly on between a Pd/Au and p-type GaN (refer to the p-type InGaN) (see fig. 1 of Mumakura et al.) to lower the resistance ohmic contacts. Thereof, the combination of Makimoto and Mumakura teaches the base electrode (Pd/Au 109 as taught by Makimoto) formed directly on said indium-containing p-type nitride semiconductor (p-type InGaN as taught by Mumakura).

Regarding **claim 81**, Makimoto discloses a nitride semiconductor structure (fig. 10) comprising: on a substrate (item 101); an n-type collector layer (item 104); a p-type



base layer (item 106) formed over said n-type collector layer (104), the p-type base layer (106) having an etched top surface (see fig.10); and an n-type emitter layer (107) formed over said p-type base layer (106).

Makimoto fails to teach an indium-containing p-type nitride layer formed directly on the etched top surface of the p-type surface.

However, Kumakura et al. suggests forming a p-type InGaN layer directly on between a metal Pd/Au layer and a p-type GaN (see pg. 2588 of Kumakura et al.: column 1, paragraph 2 and fig. 1). Therefore, it would have been obvious to one having ordinary skills in the art at the time the invention was made to insert a p-type InGaN contact layer between Pd/Au and p-type GaN as taught by Kumakura et al. in the device structure of Makimoto in order to improve the device performance by reducing the resistance contacts (see Mumakura et al.: pg. 2588; column 1, paragraph 2).

Regarding **claim 82**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Mumakura teaches said p-type nitride semiconductor layer (refer to the p-type InGaN formed between Pd/Au and p-type GaN) is p-type InGaN.

Regarding **claim 83**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Besides, Fig. 10 of Makimoto shows said p-type base layer is p-type InGaN (106).

Regarding **claim 84**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. The combination of Makimoto and Mumakura teaches said p-type nitride semiconductor layer (according to

Mumakura, the InGaN layer having In mole fraction from 0.14-0.23 as recited in col.2, line 12) has an indium mole fraction higher than an indium mole fraction of said p-type InGaN base layer (according to Makimoto, the indium mole fraction of p-InGaN base is 6% as shown in fig. 10).

Regarding **claim 85**, Makimoto and Mumakura et al. disclose all the limitations of the claimed invention for the same reasons as set-forth above. Furthermore, fig. 10 of Makimoto shows a graded layer (105) between said p-type base layer (106) and n-type collector layer (104).

### ***Conclusion***

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tram Hoang Nguyen whose telephone number is (571)272-5526. The examiner can normally be reached on Monday-Friday, 8:30 AM – 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax numbers for all communication(s) is (703)872-9306.

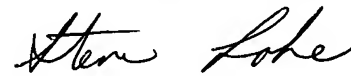
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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

**THN**  
Art Unit 2818  
10/24/2007

STEVEN LOKE  
SUPERVISORY PATENT EXAMINER

A handwritten signature in black ink, appearing to read "Steven Loke", is written below the printed name and title.